25. (Three times amended) A pre-anneal intermediate structure in the formation of an isolation structure for a semiconductor device, comprising:

a semiconductor substrate having a first surface and a second surface;

at least one p-well and at least one n-well on said substrate first surface;

at least one p-type area within said at least one n-well;

at least one n-type area within said at least one p-well; and

a substantially dopant-free, uninterrupted diffusion barrier layer extending over said [at least one p-well and said at least one n-well on said substrate] first surface and said second surface of said semiconductor substrate.

Please cancel claims 27 and 28 without prejudice or disclaimer.

33. (Amended) A pre-anneal intermediate structure in the formation of an isolation structure for a semiconductor device, comprising:

a semiconductor substrate having a first surface and a second surface;

at least one p-well and at least one n-well on said substrate first surface;

at least one doped area within at least one of said at least one n-well and said at least one p-well; and

a substantially dopant-free, uninterrupted diffusion barrier layer extending over said [at least one p-well and said at least one n-well on said substrate] first surface and said second surface of said semiconductor substrate.

Please cancel claims 35 and 36 without prejudice or disclaimer.